

Amorphous In–Ga–Zn–O Dual-Gate TFTs: Current–Voltage Characteristics and Electrical Stress Instabilities

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Abstract—We studied the electrical characteristics and electrical stress instabilities of amorphous In–Ga–Zn–O (*a*-IGZO) dual-gate thin-film-transistors (DG TFTs). A threshold voltage of the bottom-gate (BG)-driven *a*-IGZO DG TFTs showed a linear dependence on the top-gate (TG) voltage. The slope of this dependence is associated with the ratio of the TG to BG insulator capacitance. The BG-driven DG TFT showed linear field-effect mobility comparable to that of a single-gate (SG) TFT without the TG electrode and a smaller saturation field-effect mobility and a larger subthreshold swing in comparison to the SG TFT. These characteristics were explained by the BG-driven DG TFT model formulated by taking the TG bias effect into account. The TG interface showed worse stability under an electric bias stress in comparison to the BG interface. It was also found that a negative voltage applied to the TG improved the stability of the DG TFT under a constant-current stress. These observations suggest that the BG-driven *a*-IGZO DG TFTs with the appropriate negative TG voltage applied can simultaneously show both normally off characteristics and higher stability than the SG TFTs.

Index Terms—Amorphous In–Ga–Zn–O (*a*-IGZO) thin-film transistor (TFT), coplanar homojunction, dual gate, electrical stability, operation model.

I. INTRODUCTION

AMORPHOUS oxide semiconductor (AOS)-based [1] thin-film transistors (TFTs) have been extensively studied since the first demonstration of TFT operation [2]. An amorphous In–Ga–Zn–O (*a*-IGZO) TFT is one of the most promising AOS TFTs. The *a*-IGZO films can be deposited by conventional sputtering methods [3], and the TFTs show a high field-effect mobility ($> 10 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$), a low OFF-current

($< 10^{-13} \text{ A}$), and a high spatial uniformity [4]. These features have led to various prototypes of active-matrix displays based on *a*-IGZO TFTs, and their first commercial products are expected to be launched in the near future.

A dual-gate (DG) TFT has both bottom-gate (BG) and top-gate (TG) electrodes. It has been found that the *a*-IGZO DG TFTs [5]–[10] operating under DG drive (BG and TG short-circuited each other) exhibit better electrical characteristics [5], [6] and higher stabilities [6], [10] in comparison to single-(bottom)-gate (SG) TFTs. The threshold voltage of a DG TFT during BG drive can be controlled by the TG voltage, V_{TG} [7]–[9]. In the previously published papers, the operation of the DG TFTs was analyzed based on the silicon-on-insulator field-effect transistor (SOI FET) model [11], in which the channel was formed by inversion layer. However, it is not correct to apply the SOI FET model to the *a*-IGZO TFTs since the channel of the TFTs is formed by carrier accumulation.

In this paper, we studied the V_{TG} influence on the electrical characteristics of the *a*-IGZO DG TFTs with a coplanar homojunction source/drain structure [12] during the BG operation. A simple analytical model with the V_{TG} effect was formulated, and the model explained the current–voltage (I – V) characteristics of the BG-driven DG TFTs. The V_{TG} effect on the electrical stress instability was also investigated, and an appropriate negative voltage to the DG TFT improved the stability.

II. ANALYTICAL MODEL OF THE DG *a*-IGZO TFT

In this section, based on a conventional field-effect model with a gradual channel approximation [13], we formulate expressions of a drain current, i.e., I_D , for the DG TFT with an accumulation channel during the BG drive with constant V_{TG} . Fig. 1(a) shows a schematic cross section of a DG TFT with channel semiconductor (CS) thickness t_S , channel length L , and width W .

A. On Operation Region

Fig. 1(b)–(d) shows schematic cross sections of the electric states in the BG-driven DG TFT under three kinds of combination of the BG voltage, i.e., V_{BG} , and V_{TG} . When carrier electrons in the CS film of the TFT are accumulated at both the BG and TG interfaces by $V_{\text{BG}} > 0 \text{ V}$ and $V_{\text{TG}} > 0 \text{ V}$

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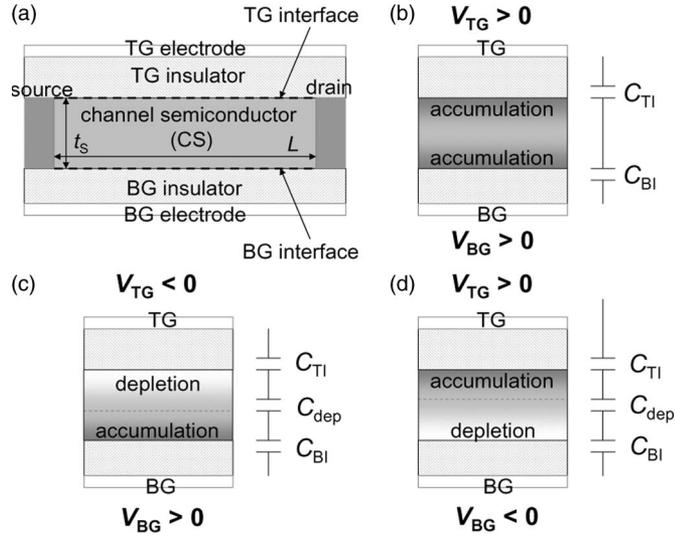


Fig. 1. Schematic cross sections of (a) a DG TFT and the electric states under on operation for (b) $V_{BG} > 0$ V and $V_{TG} > 0$ V, (c) $V_{BG} > 0$ V and $V_{TG} < 0$ V, and (d) $V_{BG} < 0$ V and $V_{TG} > 0$ V.

[see Fig. 1(b)], a charge density per unit area in the CS, i.e., Q_s , is given by

$$-Q_s = C_{BI}(V_{BG} - V_{BT0} - V) + C_{TI}(V_{TG} - V_{TT0} - V) \quad (1)$$

where C_{BI} and C_{TI} are the capacitance values per unit area of the BG and TG insulators, respectively. V is the voltage at a position, i.e., y , in the horizontal direction along the channel length from the source to the drain. V_{BT0} and V_{TT0} correspond to the threshold voltages of the SG TFT without the TG and the BG, respectively. Assuming that Q_s is equivalent to the carrier electron density in the CS film and an intrinsic drift mobility of the carrier electrons, i.e., μ_n , is constant, the voltage drop dV from y to $y + dy$ is given by

$$dV = \frac{I_D dy}{W \mu_n |Q_s|}. \quad (2)$$

Integration of (2) from $y = 0$ to $y = L$ gives I_D of the BG-driven DG TFT

$$I_D = \frac{W}{L} \mu_n C_{BI} (V_{BG} - V_{TH1}) V_D \quad (3)$$

in a linear operation region for $V_{BG} - V_{TH1} \gg V_D$ and

$$I_D = \frac{W}{2L} \frac{\mu_n C_{BI}}{C_{BI} + C_{TI}} C_{BI} (V_{BG} - V_{TH1})^2 \quad (4)$$

in a saturation operation region for $V_{BG} - V_{TH1} \leq (C_{BI} + C_{TI})V_D/C_{BI}$. In both (3) and (4), V_D is a drain voltage, and V_{TH1} is defined by

$$V_{TH1} = V_{BT0} - \frac{C_{TI}}{C_{BI}} (V_{TG} - V_{TT0}). \quad (5)$$

When $V_{BG} > 0$ V and $V_{TG} < 0$ V, a depletion layer is formed near the TG interface. The CS film becomes a double

layer composed of the depletion and the accumulation layers [7] [see Fig. 1(c)], and Q_s is given by

$$-Q_s = C_{BI}(V_{BG} - V_{BT0} - V) + \frac{C_{TI} C_{dep}}{C_{TI} + C_{dep}} (V_{TG} - V_{TT0} - V) \quad (6)$$

where C_{dep} is the depletion capacitance per area. C_{dep} is determined by the thickness of the depletion layer and larger than the CS capacitance per unit area, i.e., $C_S \equiv \epsilon_S/t_S$, where ϵ_S is the CS permittivity. When $V_{BG} < 0$ V and $V_{TG} > 0$ V, a depletion layer formed near the BG interface [see Fig. 1(d)], and Q_s is given by

$$-Q_s = \frac{C_{BI} C_{dep}}{C_{BI} + C_{dep}} (V_{BG} - V_{BT0} - V) + C_{TI} (V_{TG} - V_{TT0} - V). \quad (7)$$

The integration of (2) with Q_s in (6) and (7) also leads to I_D for $V_{BG} > 0$ V and $V_{TG} < 0$ V and for $V_{BG} < 0$ V and $V_{TG} > 0$ V, respectively.

B. Subthreshold Operation Region

The carrier electron density of the CS in the subthreshold operation region is lower than the ionized donor density, when the CS is an n-type semiconductor, such as AOS. In this region, Q_s is not equivalent to the carrier density. It is thus necessary to consider an electrostatic potential, i.e., ϕ , in the CS to determine I_D . Moreover, subgap trap states at the BG and TG interfaces and/or in the CS film influence the TFT characteristics [14], [15] because the gate-induced charge density would be lower than the trap one.

Assuming that the donor density, i.e., N_D , is constant in the CS and the densities of the BG and TG interface states per unit area per electron volt are N_{BSS} and N_{TSS} , respectively, a double integration of a Poisson equation leads to a relation, i.e.,

$$\phi_B - \phi_T = -\frac{q}{2\epsilon_S} N_D t_S^2 - \frac{\partial \phi}{\partial x} \Big|_{x=t_S} t_S \quad (8)$$

where ϕ_B and ϕ_T are potentials at the BG and TG interfaces, respectively; q is an elementary charge; and x is a position along the direction of the CS thickness from the BG to the TG interface. Using Gauss's law for the TG interface, we have

$$\frac{\partial \phi}{\partial x} \Big|_{x=t_S} = \frac{1}{\epsilon_S} \{C_{TI}(V_{TG} - V_{TFB} - \phi_T) - qN_{TSS}\phi_T\} \quad (9)$$

for $\partial \phi / \partial x|_{x=t_S}$ in (8), ϕ_T is given by

$$\phi_T = \frac{Q_D/2 + C_S \phi_B + C_{TI}(V_{TG} - V_{TFB})}{C_S + C_{TI} + C_{TSS}} \quad (10)$$

where V_{TFB} is the flatband voltage for the TG, $C_{TSS} \equiv qN_{TSS}$, and $Q_D \equiv qN_D t_S$. Substituting (10) for ϕ_T in the following equation of a charge balance is observed:

$$-(Q_D - C_{BSS}\phi_B - C_{TSS}\phi_T) = C_{BI}(V_{BG} - V_{BFB} - \phi_B) + C_{TI}(V_{TG} - V_{TFB} - \phi_T) \quad (11)$$

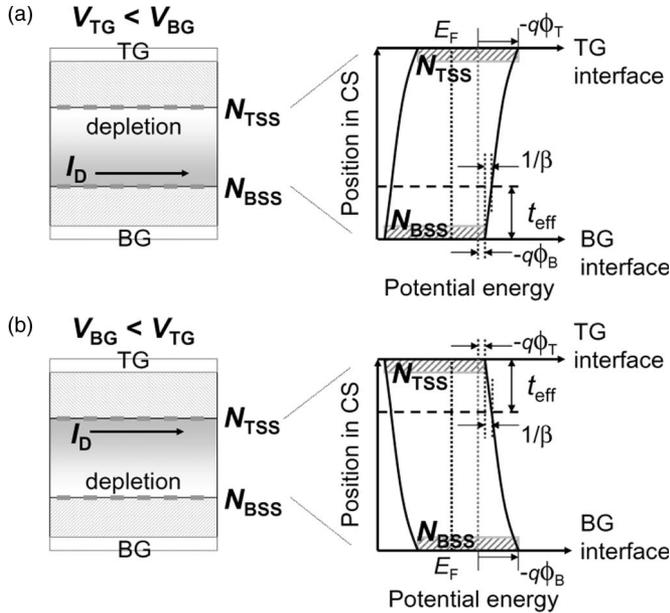


Fig. 2. Schematic cross sections of the DG TFT states and the energy state diagrams under the subthreshold operation for (a) $V_{TG} < V_{BG}$ and (b) $V_{TG} > V_{BG}$.

where V_{BFB} is the flatband voltage for the BG and $C_{BSS} \equiv qN_{BSS}$; V_{BG} is given by

$$V_{BG} = V_{BFB} - \left\{ 1 - \frac{C_{TI} + C_{TSS}}{2(C_S + C_{TI} + C_{TSS})} \right\} \frac{Q_D}{C_{BI}} + \left\{ \frac{C_{BI} + C_{BSS}}{C_{BI}} + \frac{(C_{TI} + C_{TSS})C_S}{C_{BI}(C_{TI} + C_S + C_{TSS})} \right\} \phi_B - \frac{C_{TI}C_S}{C_{BI}(C_{TI} + C_S + C_{TSS})} (V_{TG} - V_{TFB}). \quad (12)$$

Fig. 2(a) and (b) shows schematic cross sections of the electric states of the BG-driven DG TFT and the potential distribution in the CS film when $V_{BG} > V_{TG}$ and $V_{BG} < V_{TG}$, where I_D is supposed to dominantly flow near the BG and TG interfaces, respectively. We assume that a carrier density per unit area is determined by a product of the carrier electron density at the interface and an effective channel thickness for drain current flow [13]. The effective channel thickness, i.e., t_{eff} , is defined as a distance from the interface, at which the electrostatic potential decreases by $k_B T/q = 1/\beta$ with Boltzmann's constant k_B and absolute temperature T . Using Boltzmann's statistics, t_{eff} near the BG interface is given by

$$t_{eff} = \frac{1}{\beta E_s} = \frac{1}{\beta} \left(\frac{\partial \phi}{\partial x} \Big|_{x=0} \right)^{-1} \quad (13)$$

where E_s is an electric field at the BG interface. Using (13), I_D near the BG interface in the subthreshold region is given by

$$I_D \sim \mu_n \frac{W}{L} \frac{1 - e^{-\beta V_D}}{\beta^2} \left(\frac{\partial \phi}{\partial x} \Big|_{x=0} \right)^{-1} n_{e0} e^{\beta \phi_B} \quad (14)$$

where n_{e0} is a carrier electron density under flatband condition. Applying Gauss's law to the BG interface, i.e.,

$$\frac{\partial \phi}{\partial x} \Big|_{x=0} = -\frac{1}{\epsilon_S} \{ C_{BI}(V_{BG} - V_{BFB} - \phi_B) - C_{BSS}\phi_B \} \quad (15)$$

for $\partial \phi / \partial x|_{x=0}$ in (14) gives a representation of S under the BG drive by

$$S \equiv \frac{\partial V_{BG}}{\partial \log(I_D)} \sim \frac{\ln 10}{\beta} \left(\frac{\partial \phi_B}{\partial V_{BG}} \right)^{-1} \times \left\{ 1 - \frac{1}{\beta} \frac{C_{BI}(\partial \phi_B / \partial V_{BG})^{-1} - (C_{BI} + C_{BSS})}{C_{BI}(V_{BG} - V_{BFB}) - (C_{BI} + C_{BSS})\phi_B} \right\}^{-1} \sim \frac{\ln 10}{\beta} \left(\frac{\partial \phi_B}{\partial V_{BG}} \right)^{-1} \quad (16)$$

where the last approximation is from the evaluation of

$$\left| \frac{1}{\beta \phi_B} \frac{C_{BI}(\partial V_{BG} / \partial \phi_B) - (C_{BI} + C_{BSS})}{C_{BI}(V_{BG} - V_{BFB}) / \phi_B - (C_{BI} + C_{BSS})} \right| \ll 1 \quad (17)$$

with $1/\beta \sim 26$ meV at room temperature (RT). From (12) and (16), S for $V_{BG} > V_{TG}$ is given by

$$S \sim \frac{\ln 10}{\beta} \left[\frac{C_S(C_{TI} + C_{TSS})}{C_{BI}(C_S + C_{TI} + C_{TSS})} + \frac{C_{BI} + C_{BSS}}{C_{BI}} \right]. \quad (18)$$

S for $V_{TG} > V_{BG}$ [see Fig. 2(b)] is also derived by the similar procedure.

C. Comparison With a Conventional TFT Model

A conventional model of the SG TFT gives I_D in a linear region for $V_{BG} - V_{TH} \gg V_D$, i.e.,

$$I_D = \frac{W}{L} \mu_{lin} C_{BI} (V_{BG} - V_{TH}) V_D \quad (19)$$

and I_D in a saturation region for $V_{BG} - V_{TH} < V_D$, i.e.,

$$I_D = \frac{W}{2L} \mu_{sat} C_{BI} (V_{BG} - V_{TH})^2 \quad (20)$$

where V_{TH} is a threshold voltage, and μ_{lin} and μ_{sat} are a linear and a saturation field-effect mobility (hereinafter called linear and saturation mobility, respectively). When interface traps of $N_{BSS} = C_{BSS}/q$ and $N_{TSS} = C_{TSS}/q$ near the BG and the TG interface, S is given by

$$S \sim \frac{\ln 10}{\beta} \left(1 + \frac{C_{BSS} + C_{TSS}}{C_{BI}} \right). \quad (21)$$

From Sections II-A and II-B, I_D of the DG TFT under the BG drive with constant V_{TG} in the on operation region is given by

$$I_D = \frac{W}{L} \mu_n C'_{BI} (V_{BG} - V_{TH}) V_D \quad (22)$$

in a linear operation region for $V_{BG} - V_{TH} \gg V_D$ or

$$I_D = \frac{W}{2L} \frac{\mu_n C'_{BI}}{C'_{BI} + C'_{TI}} C'_{BI} (V_{BG} - V_{TH})^2 \quad (23)$$

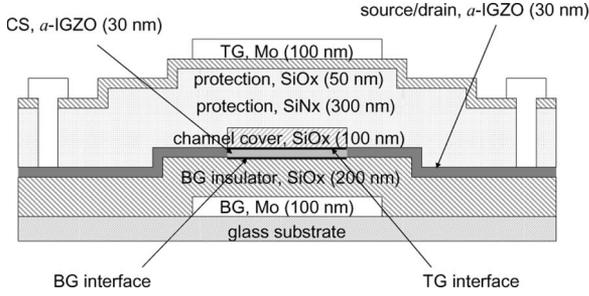


Fig. 3. Schematic cross section of the coplanar homojunction *a*-IGZO DG TFT.

in a saturation operation region for $V_{BG} - V_{TH} \leq (C'_{BI} + C'_{TI})V_D/C'_{BI}$, where V_{TH} is given by

$$V_{TH} = V_{BT0} - \frac{C'_{TI}}{C'_{BI}}(V_{TG} - V_{TT0}) \quad (24)$$

and C'_{BI} and C'_{TI} are given by

$$C'_{BI}, C'_{TI} = \begin{cases} C_{BI}, C_{TI} & \text{(a)} \\ C_{BI}, \frac{C_{TI}C_{dep}}{C_{TI} + C_{dep}} & \text{(b)} \\ \frac{C_{BI}C_{dep}}{C_{BI} + C_{dep}}, C_{TI} & \text{(c)} \end{cases} \quad (25)$$

for (a) $V_{BG}, V_{TG} > 0$, (b) $V_{BG} > 0$ and $V_{TG} < 0$, and (c) $V_{BG} < 0$ and $V_{TG} > 0$, respectively. In the subthreshold region, S of the BG-driven DG TFT is given by

$$S \sim \begin{cases} \frac{\ln 10}{\beta} \left[\frac{C_S(C_{TI} + C_{TSS})}{C_{BI}(C_S + C_{TI} + C_{TSS})} + \frac{C_{BI} + C_{BSS}}{C_{BI}} \right] \\ \frac{\ln 10}{\beta} \left[\frac{(C_{BI} + C_{BSS})(C_S + C_{TI} + C_{TSS})}{C_{BI}C_S} + \frac{C_{TI} + C_{TSS}}{C_{BI}} \right] \end{cases} \quad (26)$$

for $V_{BG} < V_{TG}$ and for $V_{BG} > V_{TG}$, respectively.

III. EXPERIMENTAL SECTION

The coplanar homojunction *a*-IGZO SG and DG TFTs were fabricated by the same process sequence as described in [12], and a Mo TG electrode was formed on only the top of the DG TFT. Fig. 3 shows the schematic cross section of the *a*-IGZO DG TFT.

We measured current–voltage (I – V) characteristics of the BG-driven SG and DG TFTs with $W/L = 60/10 \mu\text{m}$, at $V_D = 0.1$ and 12 V, respectively. To investigate the V_{TG} effects on the I – V characteristics of the DG TFT, $V_{TG} = -10, -5, 0, 5,$ and 10 V were applied to the DG TFT during the measurement. The TFTs were subjected to two kinds of instability tests. (i) A constant-current stress with constant $V_{BG} = V_D$ and a source voltage, i.e., V_S , varied so as to keep a drain current of $I_D = 4 \mu\text{A}$ for 10^4 s was applied to the TFTs. Under the current stress test, a change in $V_{BG} - V_S$ was analyzed as V_{TH} variation, ΔV_{TH} . (ii) A constant-voltage stress with low V_D and high V_{BG} (or V_{TG}) for 3000 s was applied to the TFTs. All the electrical characteristics and electrical stress instabilities were measured using a precision semiconductor parameter analyzer (Agilent 4156C) in the dark at RT. The source electrode of the TFTs was grounded during the measurements except the constant-current instability tests.

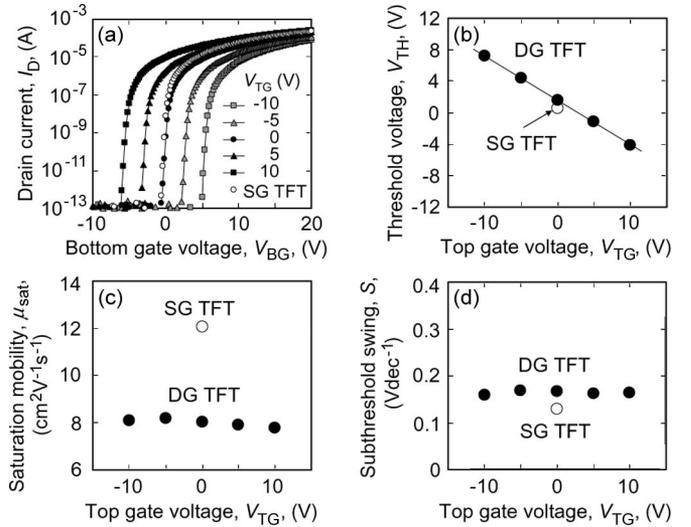


Fig. 4. V_{TG} dependence of I – V characteristics of the SG and the BG-driven TFTs: (a) transfer curves at $V_D = 12$ V and various V_{TG} , (b) V_{TH} , (c) μ_{sat} , and (d) S . Open and closed symbols stand for the results of the SG TFT and the BG-driven DG TFT, respectively.

TABLE I
TFT PARAMETERS OF THE *a*-IGZO SG TFT AND THE BG-DRIVEN *a*-IGZO DG TFT AT $V_D = 0.1$ AND 12 V

V_D	parameter	unit	SG	DG
0.1 V	threshold voltage, V_{TH}	V	2.69	2.58
	linear mobility, μ_{lin}	$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$	12.5	12.4
	subthreshold swing, S	V dec^{-1}	0.15	0.17
12 V	threshold voltage, V_{TH}	V	1.43	1.72
	saturation mobility, μ_{sat}	$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$	12.2	8.21
	subthreshold swing, S	V dec^{-1}	0.13	0.17

In this paper, TFT parameters of all the TFTs were extracted by the following method. S was defined as $\partial V_{BG} / \partial \log I_D$ at $I_D = 0.1$ nA. V_{TH} and an apparent linear mobility, i.e., μ_{lin} , in the linear operation region were derived from a linear fitting to the transfer curve at $V_D = 0.1$ V using (19). V_{TH} and an apparent saturation mobility, i.e., μ_{sat} , in the saturation operation region were derived from a linear fitting to the $\sqrt{I_D} - V_G$ curve at $V_D = 12$ V using (20).

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. DG TFT I – V Characteristics

Fig. 4(a) shows transfer curves of the *a*-IGZO SG TFT and the BG-driven *a*-IGZO DG TFT at $V_D = 12$ V and various V_{TG} . The application of V_{TG} simply shifts the transfer curves to the larger V_{BG} direction. Table I shows extracted TFT parameters, and μ_{sat} of the BG-driven DG TFT is apparently smaller than μ_{lin} of the SG TFT and the BG-driven DG TFT and μ_{sat} of the SG TFT. The BG-driven DG TFT showed a larger S than that of the SG TFT.

1) *Threshold Voltage*: Fig. 4(b) shows V_{TG} dependence of V_{TH} . V_{TH} of the BG-driven *a*-IGZO DG TFT can be regarded as a linear function of V_{TG} , and the linear dependence is observed in a wide range from negative to positive V_{TG} .

Because the DG TFT satisfies $C_{dep} \gg C_{BI}, C_{TI}$, (24) both for $V_{BG} > 0$ V and $V_{TG} < 0$ V and for $V_{BG} < 0$ V and $V_{TG} >$

0 V can be approximated into an equation of

$$V_{TH} \sim V_{BT0} - \frac{C_{TI}}{C_{BI}}(V_{TG} - V_{T0}). \quad (27)$$

Equation (27) discusses V_{TH} of the BG-driven DG TFT for V_{TG} ranging from negative to positive value with a slope of $-C_{TI}/C_{BI}$. The result shown in Fig. 4(b) indicates that the slope of V_{TH} is -0.56 and close to $-C_{TI}/C_{BI} = -0.59$ calculated from the structure of the DG TFT. The same linear relation expressed by (27) was also observed for the a -IGZO DG TFTs having the other structures, such as coplanar homojunction DG TFTs with thicker TG insulators, top-contact S/D DG TFTs, and bottom-contact S/D DG TFTs [8].

Equation (27) is mathematically equivalent to the expression of V_{TH} given by the SOI FET model [11]. The SOI FET model needs the depletion layer and the negative V_{TG} . On the other hand, (27) is valid for the a -IGZO DG TFT with or without the depletion layer since the on operation is induced by the accumulation of carrier electrons. This feature expands the range of the linear dependence of V_{TH} on V_{TG} from negative to positive V_{TG} , as shown in Fig. 4(b).

There are three cases for which V_{TH} cannot be represented by (27). The first is the case of thicker a -IGZO films that do not satisfy the condition of $C_{dep} \gg C_{BI}$, C_{TI} , and V_{TH} should be given by (24). The second case is when the subgap trap-state density in the a -IGZO film is high. The electric field from the TG is, then, shielded by the positive ionized trap states, and the influence of the field at the BG interface becomes smaller. As a result, the V_{TG} dependence of V_{TH} decreases or even disappears. This consideration suggests that the subgap trap-state density in the a -IGZO is low because of the V_{TH} linear dependence with the slope of $-C_{TI}/C_{BI}$. A gradual slope of V_{TH} shift ($\partial V_{TH}/\partial V_{TG}$) for the BG-driven a -Si:H DG TFT with $V_{TG} < 0$ V [7] could be explained by this mechanism. The third case is that holes are accumulated near the TG interface in the a -IGZO channel. The electric field from the TG is, then, shielded by the accumulated holes, and the $|\partial V_{TH}/\partial V_{TG}|$ value is reduced as in SOI FETs [11]. So far, a formation of a hole accumulation layer has not been observed in a -IGZO TFTs, probably because (i) the hole injection rate from the source/drain electrodes is very low due to the deep valence band level [16] and the low hole mobility of a -IGZO [17], and (ii) the high-density traps above the valence band maximum pin the Fermi level [14].

2) *Field-Effect Mobility*: Fig. 4(c) shows a relation between V_{TG} and μ_{sat} for the BG-driven DG TFT at $V_D = 12$ V, and μ_{sat} of the SG TFT is also shown at $V_{TG} = 0$ V. As shown in Fig. 4(c) and Table I, μ_{sat} of the DG TFT ($\sim 8.0 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ on average for $-10 \leq V_{TG} \leq 10$ V) is independent of V_{TG} and smaller than that of the SG TFT or μ_{lin} of both the SG and DG TFTs.

Since (19) and (22) have the same formula, μ_n in the BG-driven DG TFT model is equal to μ_{lin} in the conventional model. From comparison between (20) and (23), we can extract the following relationship:

$$\mu_{sat} = \frac{C_{BI}}{C_{BI} + C_{TI}} \mu_n = \frac{C_{BI}}{C_{BI} + C_{TI}} \mu_{lin}. \quad (28)$$

With $C_{BI}/(C_{BI} + C_{TI}) = 0.63$ calculated for our device structure and $\mu_{lin} = 12.4 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ of the DG TFT (see Table I), (28) predicts $\mu_{sat} = 7.8 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$, which is very close to $8.0 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ averaged over the measured values.

It is well known that a -IGZO TFTs often show nonlinearity in I - V characteristics under the on operation [18], [19]. The simple model of the BG-driven DG TFT in this study does not include the nonlinearity but explains well the characteristics as seen above. We confirmed that the model with the nonlinearity can be formulated by using the bias-dependent mobility [19] and shows almost the same V_{TG} dependence of V_{TH} and the mobility relation between the SG and the BG-driven DG TFTs as those of the simple model.

3) *Subthreshold Swing*: Fig. 4(d) shows a relation between V_{TG} and S , where S is independent of V_{TG} .

If $C_S \gg \forall C \in \{C_{BI}, C_{TI}, C_{BSS}, C_{TSS}\}$ is satisfied, (26) consisting of two expressions for $V_{BG} > V_{TG}$ and $V_{BG} < V_{TG}$ can be further approximated into an equation of

$$S \sim \frac{\ln 10}{\beta} \left(1 + \frac{C_{TI} + C_{BSS} + C_{TSS}}{C_{BI}} \right). \quad (29)$$

There is the term of C_{TI}/C_{BI} in the bracket of (29). Therefore, the BG-driven DG TFT essentially should exhibit a larger S than the SG TFT.

Assuming $C_{BSS} = C_{TSS}$ for convenience, $N_{BSS} \sim 7.3 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ is extracted from measured $S = 0.17 \text{ V} \cdot \text{dec}^{-1}$ of the BG-driven DG TFT by (29). With this N_{BSS} , S of the SG TFT can be estimated by (21) as $S \sim 0.14 \text{ V} \cdot \text{dec}^{-1}$, which is almost the same as the measured value of $0.13 \text{ V} \cdot \text{dec}^{-1}$ (see Table I).

B. DG TFT Instability

We also studied electrical instabilities of the a -IGZO SG and DG TFTs under the constant-current stress [20], [21] and the constant-voltage stress tests at RT.

Fig. 5(a) shows a relation between V_{BG} and V_{TG} to realize constant current of $I_D = 4 \mu\text{A}$ with $V_{BG} = V_D$. To keep I_D constant, V_{BG} decreases with the increase in V_{TG} . The slope of $\partial V_{BG}/\partial V_{TG}$ is about -0.6 , which is almost the same as the calculated $-C_{TI}/C_{BI} = -0.59$, indicating that the simple analytical model developed in this study is consistent with the observed relation. Fig. 5(b) shows ΔV_{TH} during the constant-current stress of $4 \mu\text{A}$ with $V_{BG} = V_D$. The values of ΔV_{TH} were smaller than 0.1 V and are consistent with the previously reported values in [20]. Fig. 5(c) shows the dependence of ΔV_{TH} on V_{TG} under the constant-current stress for 10^4 s. The V_{TG} dependence of ΔV_{TH} can be approximated by a quadratic polynomial function of V_{TG} , i.e.,

$$\Delta V_{TH} = 1.71 \times 10^{-3} V_{TG}^2 + 5.96 \times 10^{-3} V_{TG} + 3.72 \times 10^{-2} \quad (30)$$

shown by the dotted line in Fig. 5(b), which exhibits the minimum of 0.03 V at $V_{TG} = -1.7$ V.

Electrical instability of the SG TFT and the BG-driven DG TFTs under the constant-voltage stress were also measured.

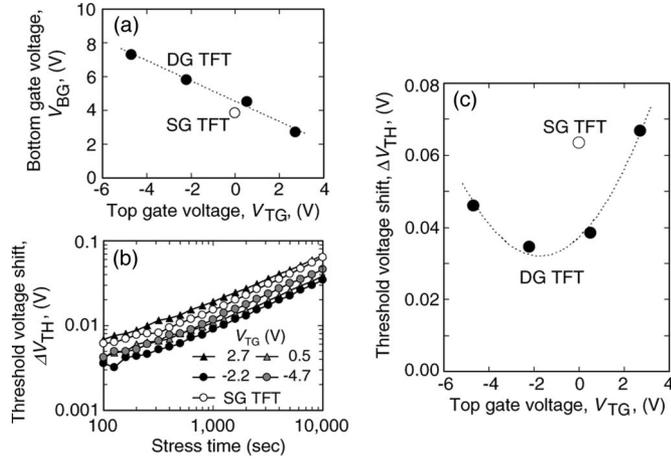


Fig. 5. V_{TG} dependence of V_{BG} and ΔV_{TH} in $4\text{-}\mu\text{A}$ constant-current stress tests: (a) V_{BG} to induce I_D of $4\text{ }\mu\text{A}$, (b) ΔV_{TH} variations during the test, and (c) ΔV_{TH} by the test for 10^4 s. Open and closed symbols stand for the results of the SG and the DG TFTs, respectively.

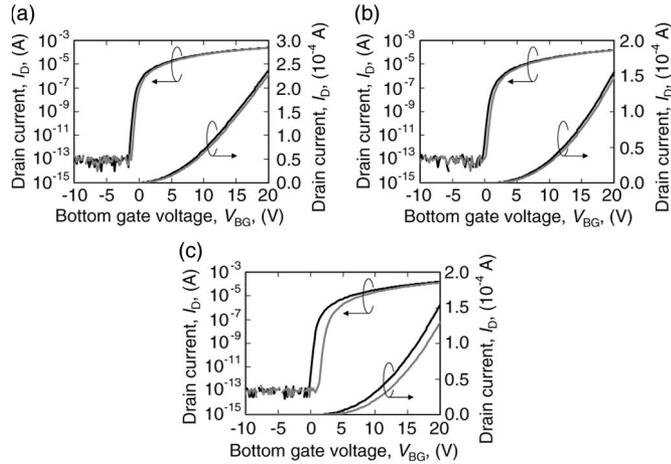


Fig. 6. Transfer curves at $V_D = 12$ V before and after constant-voltage stress tests for 3000 s: (a) curves of the SG TFT before and after the stress at $V_{BG} = 20$ and $V_D = 0.1$ V; (b) curves of the BG-driven DG TFT before and after the stress at $V_{BG} = 20$, $V_D = 0.1$, and $V_{TG} = 0$ V; and (c) curves of the BG-driven DG TFT before and after the stress at $V_{BG} = 0$, $V_D = 0.1$, and $V_{TG} = 20$ V.

Fig. 6(a) and (b) shows transfer curves of the SG TFT and the BG-driven DG TFTs at $V_D = 12$ V before and after the constant-voltage stress at $V_{BG} = 20$ V, $V_D = 0.1$ V, and $V_{TG} = 0$ V for 3000 s, respectively. The stress led to $\Delta V_{TH} = 0.4$ V with little variation in μ_{sat} and S in both the SG and the BG-driven DG TFTs. Such changes in the transfer curves are consistent with the filling of trap states with electrons induced by V_{BG} near the BG interface. The energy level of the traps is deeper than -0.8 eV [15] below the conduction band minimum because μ_{sat} and S did not change during the stress. When the constant-voltage stress was applied to the TG electrode of the DG TFT at $V_{TG} = 20$ V, $V_D = 0.1$ V, and $V_{BG} = 0$ V for 3000 s, ΔV_{TH} was about 1.5 V with little variation in μ_{sat} and S [see Fig. 6(c)]. The TG voltage stress caused the larger ΔV_{TH} than the BG voltage stress in spite of the smaller capacitance of the TG insulator in comparison to the BG insulator. These results suggest that trap states near the TG interface have higher density than those near the BG

interface. The high trap density near the TG interface would lead to the ΔV_{TH} minimum at $V_{TG} = -1.7$ V for the constant-current stress because the negative V_{TG} suppresses the electron density near the TG interface.

It is highly possible that the deposition of the channel-cover SiO_x film causes some damage onto the top surface of the a -IGZO film, which could increase the trap density near the TG interface. Although the density could be reduced by improving the deposition methods of the top insulator film or by post thermal annealing, it is difficult for these approaches to reverse the relation between the trap densities near the TG and the BG interfaces. We believe, therefore, that electrical stability of the DG TFTs can be improved by applying an appropriate negative voltage to the TG electrode, and at the end, electrical stability of the DG TFT is expected to be better than that of the SG TFTs.

V. CONCLUSION

We investigated V_{TG} influence on I - V characteristics and electrical-stress-induced instabilities of the a -IGZO DG TFTs with a coplanar homojunction structure in comparison to the SG TFTs. The threshold voltage of the BG-driven DG TFT linearly depended on V_{TG} , with a slope close to $-C_{TI}/C_{BI}$. The BG-driven DG TFT showed a linear field-effect mobility comparable to that of the SG TFT, while the saturation field-effect mobility was $C_{BI}/(C_{BI} + C_{TI})$ times smaller than that of the SG TFT. The subthreshold swing of the BG-driven DG TFT was slightly larger than that of the SG TFT. These characteristics were explained by a simple analytical model taking into account the effect of the TG bias. The constant-voltage stress tests of SG and DG TFTs showed that the TG interface was less stable than the BG interface. The instability near the TG interface could be the origin of the V_{TG} influence on the device stability under the constant-current stress with the highest stability observed at $V_{TG} = -1.7$ V. The BG-driven a -IGZO DG TFTs with an appropriate V_{TG} applied can show both normally off characteristics and a high stability in comparison to conventional SG TFTs.

APPENDIX MODEL FOR DG-DRIVEN DG TFT

This appendix shows a model for DG-driven DG TFTs based on the model for the BG-driven DG TFTs in Section II.

When $V_{TG} = V_{BG}$ and $V_{TT0} = V_{BT0}$, (3) for the linear operation becomes

$$I_D = \frac{W}{L} \mu_n (C_{BI} + C_{TI}) (V_{BG} - V_{BT0}) V_D \quad (\text{A1})$$

and (4) for the saturation operation becomes

$$I_D = \frac{W}{L} \mu_n (C_{BI} + C_{TI}) \frac{(V_{BG} - V_{BT0})^2}{2}. \quad (\text{A2})$$

Based on the similar approach to derive (29), S for the DG-driven DG TFT is approximated by

$$S \sim \frac{\ln 10}{\beta} \left(1 + \frac{C_{BSS} + C_{TSS}}{C_{BI} + C_{TI}} \right). \quad (\text{A3})$$

Equations (A1)–(A3) indicate that the on and the subthreshold operations of the DG-driven DG TFT are the same as those of the SG TFT having a gate capacitance per unit area of $C_{BI} + C_{TI}$, respectively.

We applied the model to coplanar homojunction α -IGZO TG-, BG-, and DG-driven DG TFTs [22]. The model for the TG-driven DG TFT is obtained by replacing the index “B” with “T” (and “T” with “B”) of the model for the BG-driven DG TFT. I_{ON} of the DG-driven DG TFT in the linear on operation region (2.0×10^{-6} A) is almost close to the sum of I_{ON} of the TG-driven DG TFT (6.3×10^{-7} A) and I_{ON} of the BG-driven DG TFT (1.3×10^{-6} A) [see eqs. (22) and (A1)]. From the model [see eqs. (23) and (A2)], I_{ON} of the TG- and BG-driven DG TFT, i.e., $I_{ON}(TG)$ and $I_{ON}(BG)$, in the saturated on operation region are represented by

$$\begin{aligned} I_{ON}(TG) &\sim \left(\frac{C_{TI}}{C_{BI} + C_{TI}} \right)^2 I_{ON}(DG) \\ &= 1.3 \times 10^{-5} \text{ A} \end{aligned} \quad (\text{A4})$$

$$\begin{aligned} I_{ON}(BG) &\sim \left(\frac{C_{BI}}{C_{BI} + C_{TI}} \right)^2 I_{ON}(DG) \\ &= 4.7 \times 10^{-5} \text{ A} \end{aligned} \quad (\text{A5})$$

where $I_{ON}(DG)$ is I_{ON} of the DG-driven DG TFT (1.1×10^{-4} A). These estimations are almost the same as the measured values. The model [see eqs. (29) and (A3)] leads to similar $N_{SS} = N_{BSS} = N_{TSS}$ from S values in [22] as

$$N_{SS}(TG) \sim 6.0 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1} \quad (S=0.29 \text{ V} \cdot \text{dec}^{-1})$$

$$N_{SS}(BG) \sim 5.4 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1} \quad (S=0.15 \text{ V} \cdot \text{dec}^{-1})$$

$$N_{SS}(DG) \sim 5.8 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1} \quad (S=0.10 \text{ V} \cdot \text{dec}^{-1})$$

respectively. We consider that these observations support the validity of the DG TFT model described in this paper.

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